FIG. 1

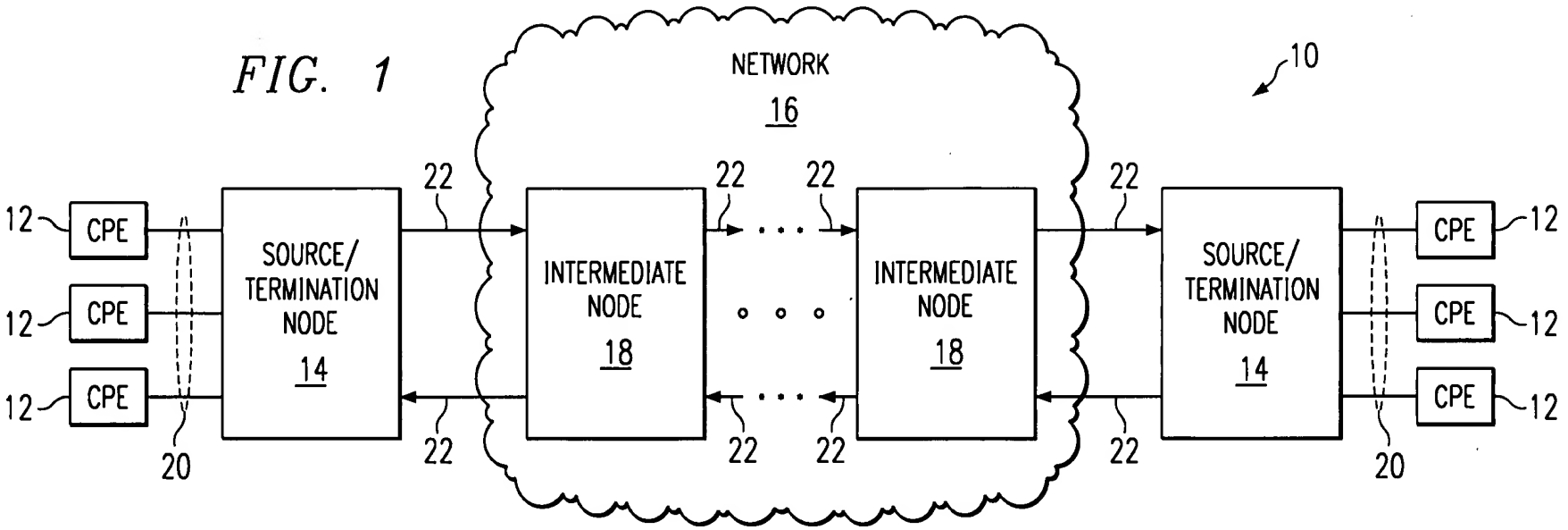
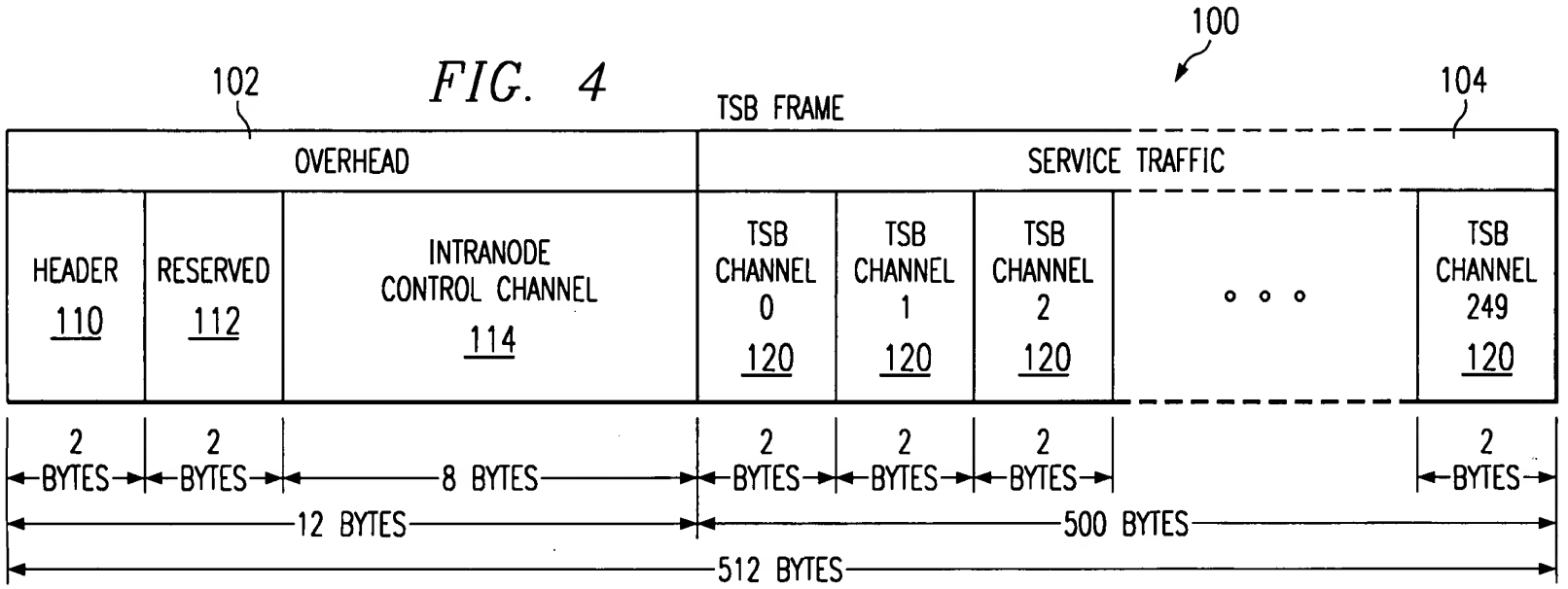


FIG. 4



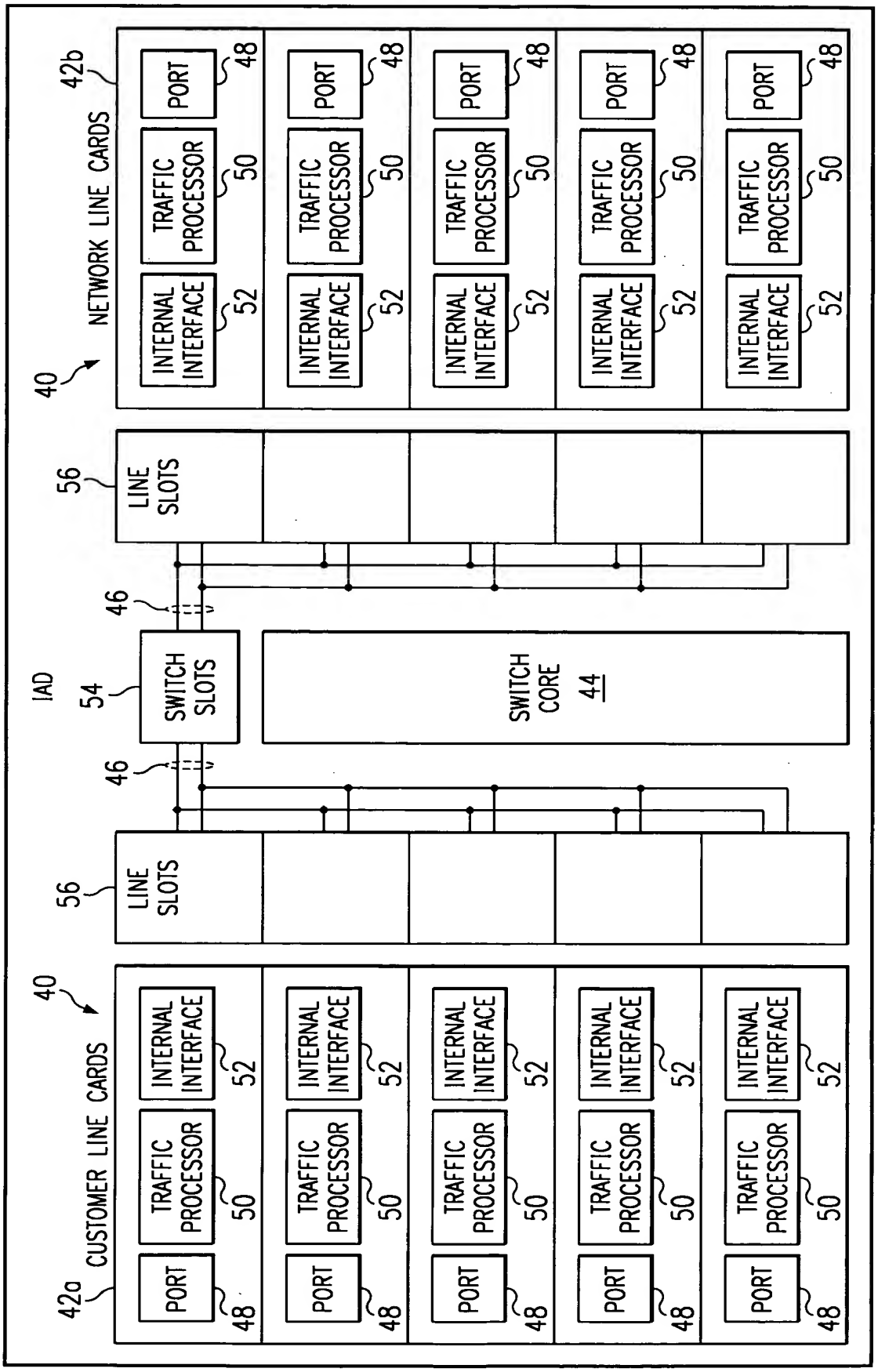

14
IAD
40
CUSTOMER LINE CARDS
42a
40
NETWORK LINE CARDS
42b
PORT
48
TRAFFIC PROCESSOR
50
INTERNAL INTERFACE
52
LINE SLOTS
56
SWITCH SLOTS
54
SWITCH CORE
44
46

FIG. 2

FIG. 3

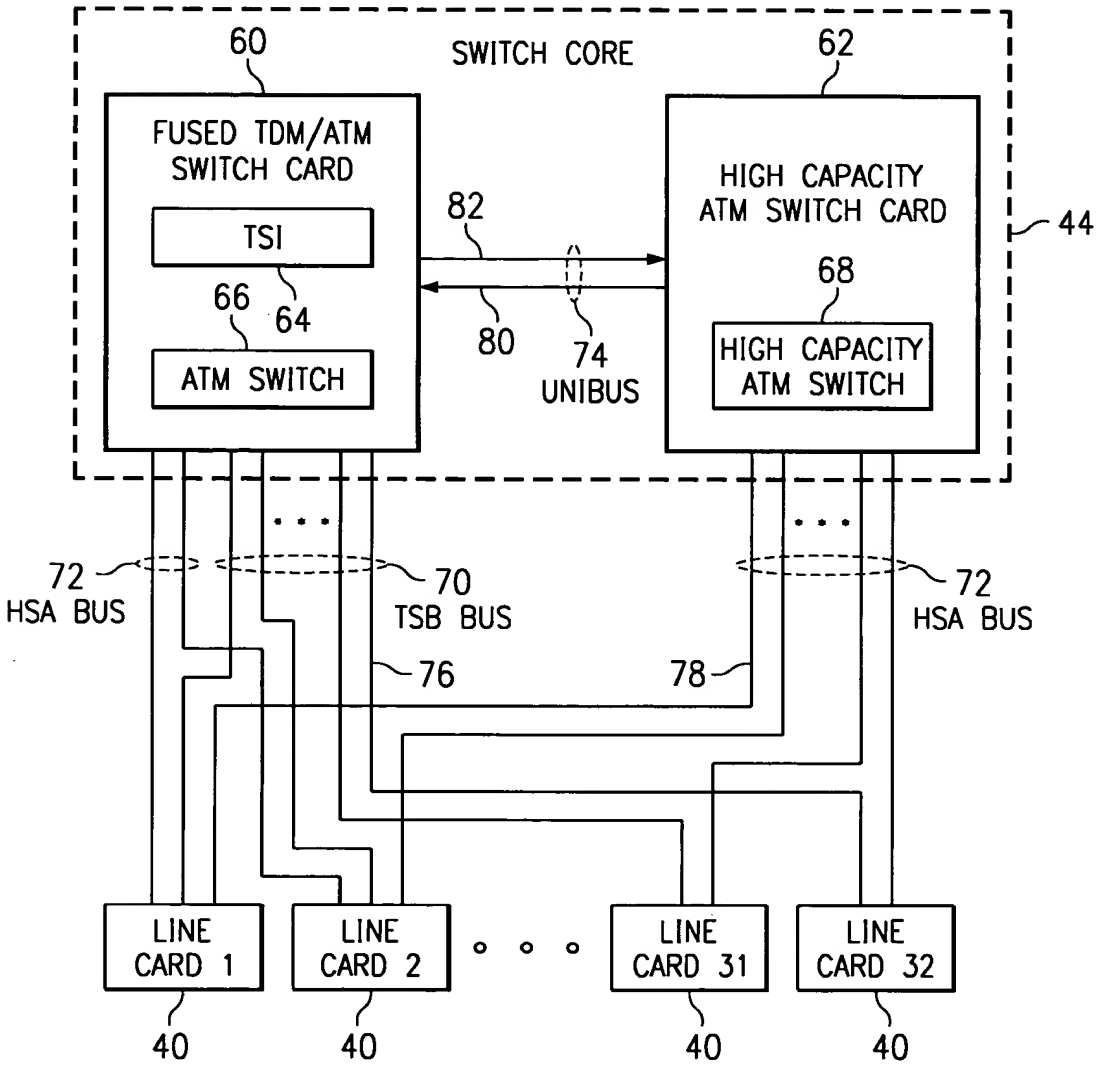
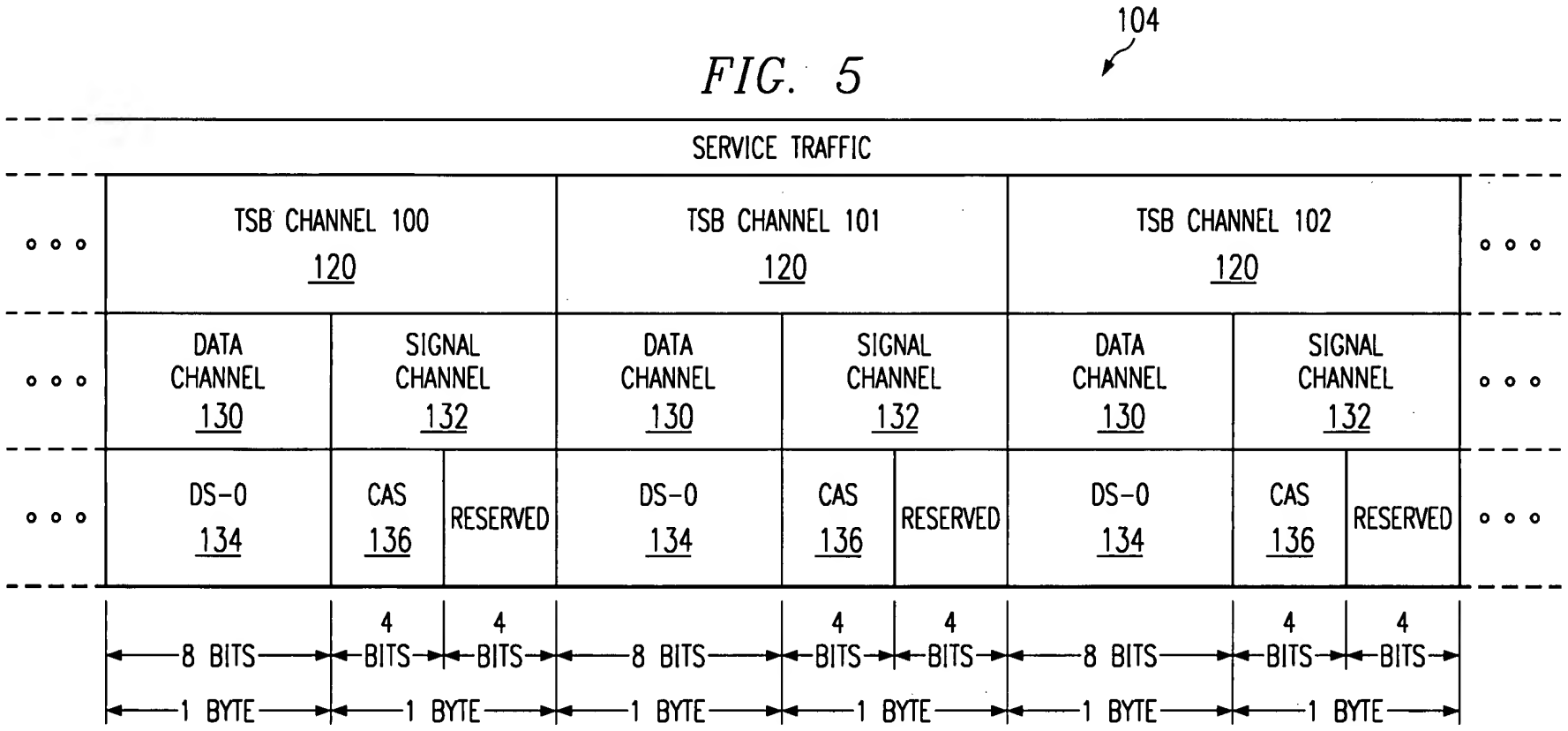

60
SWITCH CORE
62
FUSED TDM/ATM SWITCH CARD
TSI
66
64
ATM SWITCH
82
80
74
UNIBUS
HIGH CAPACITY ATM SWITCH CARD
68
HIGH CAPACITY ATM SWITCH
44
72
HSA BUS
70
TSB BUS
72
HSA BUS
76
78
LINE CARD 1
LINE CARD 2
LINE CARD 31
LINE CARD 32
40
40
40
40

FIG. 5



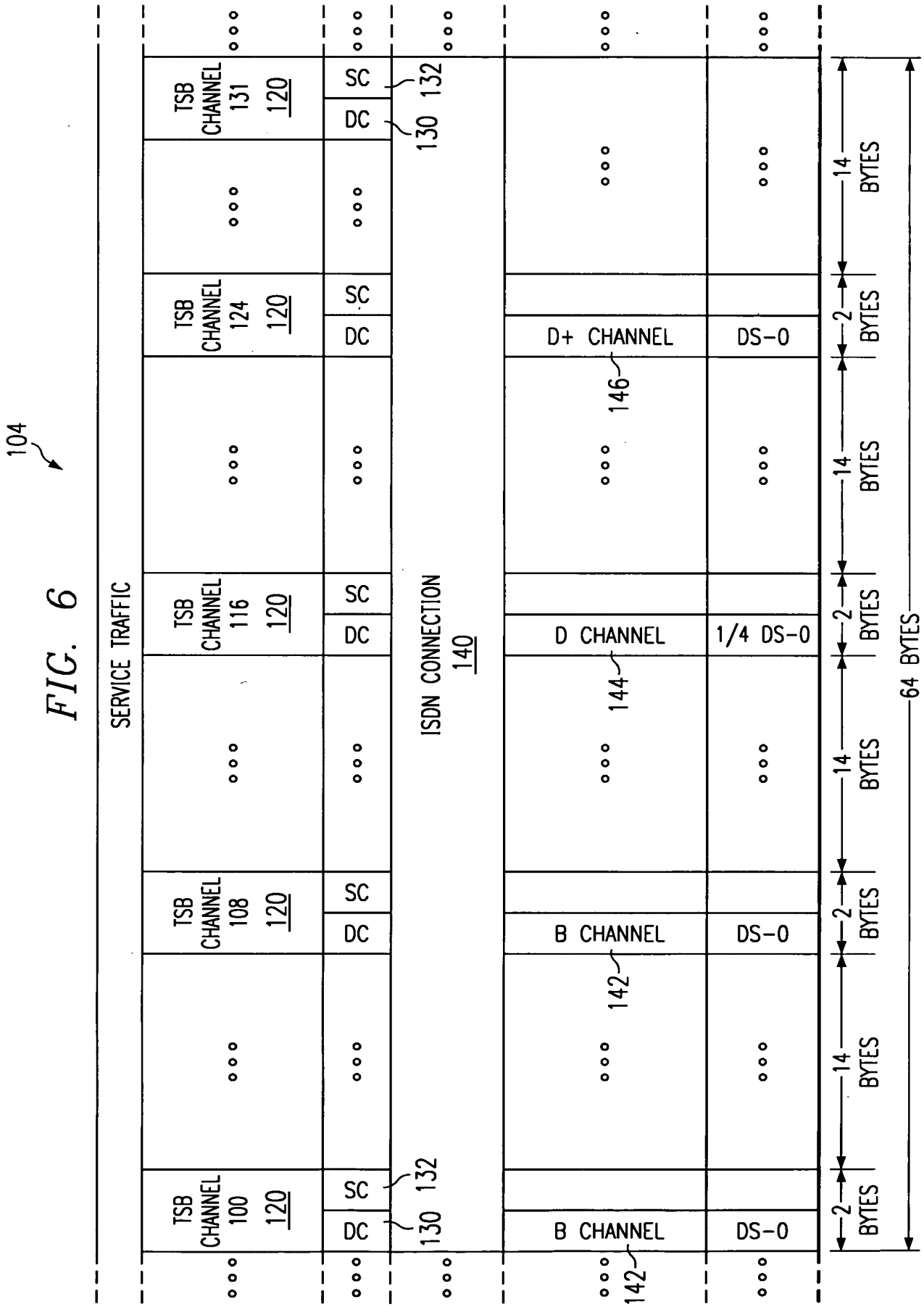

104
SERVICE TRAFFIC
TSB CHANNEL 100 120
TSB CHANNEL 108 120
TSB CHANNEL 116 120
TSB CHANNEL 124 120
TSB CHANNEL 131 120
SC
DC
130 132
ISDN CONNECTION 140
B CHANNEL
D CHANNEL
D+ CHANNEL
DS-0
1/4 DS-0
142
144
146
2 BYTES
14 BYTES
64 BYTES

FIG. 6

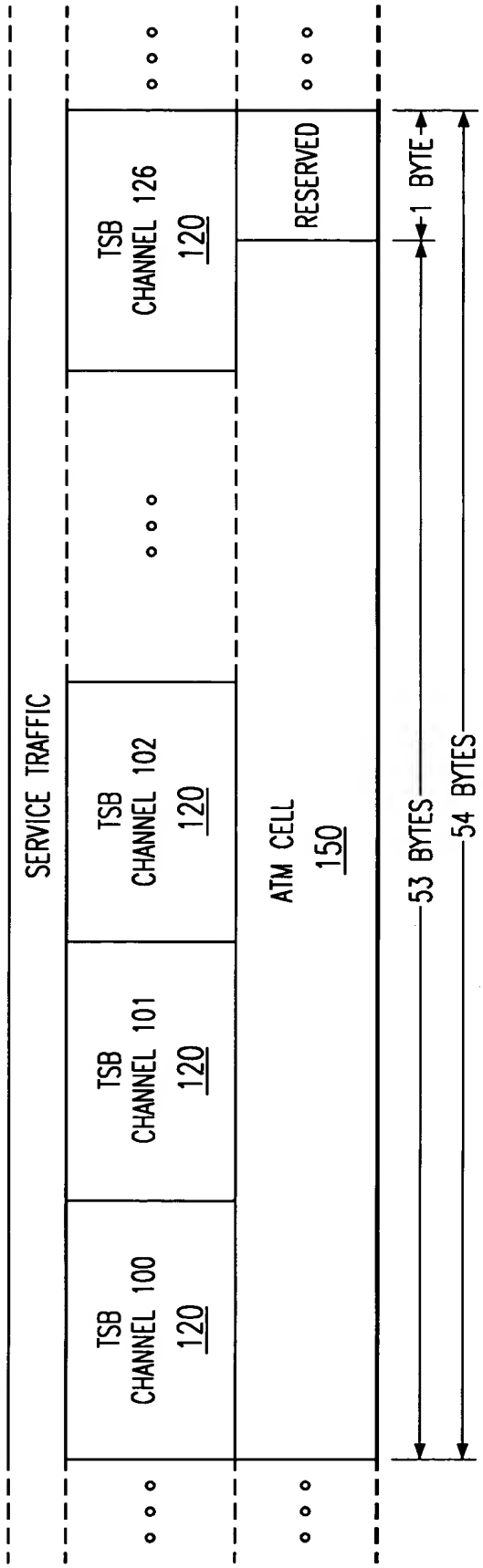

104
SERVICE TRAFFIC
TSB CHANNEL 100 120
TSB CHANNEL 101 120
TSB CHANNEL 102 120
TSB CHANNEL 126 120
RESERVED
ATM CELL 150
1 BYTE
53 BYTES
54 BYTES

FIG. 7

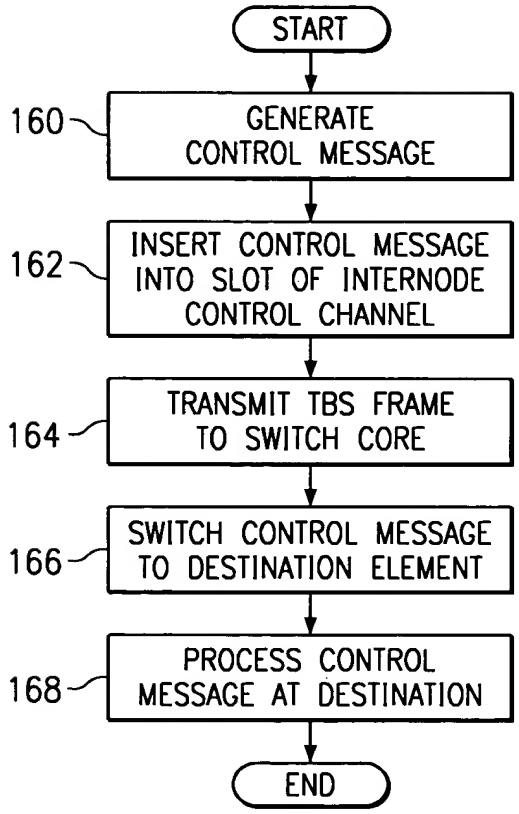

START
160
GENERATE CONTROL MESSAGE
162
INSERT CONTROL MESSAGE INTO SLOT OF INTERNODE CONTROL CHANNEL
164
TRANSMIT TBS FRAME TO SWITCH CORE
166
SWITCH CONTROL MESSAGE TO DESTINATION ELEMENT
168
PROCESS CONTROL MESSAGE AT DESTINATION
END

FIG. 8

FIG. 9

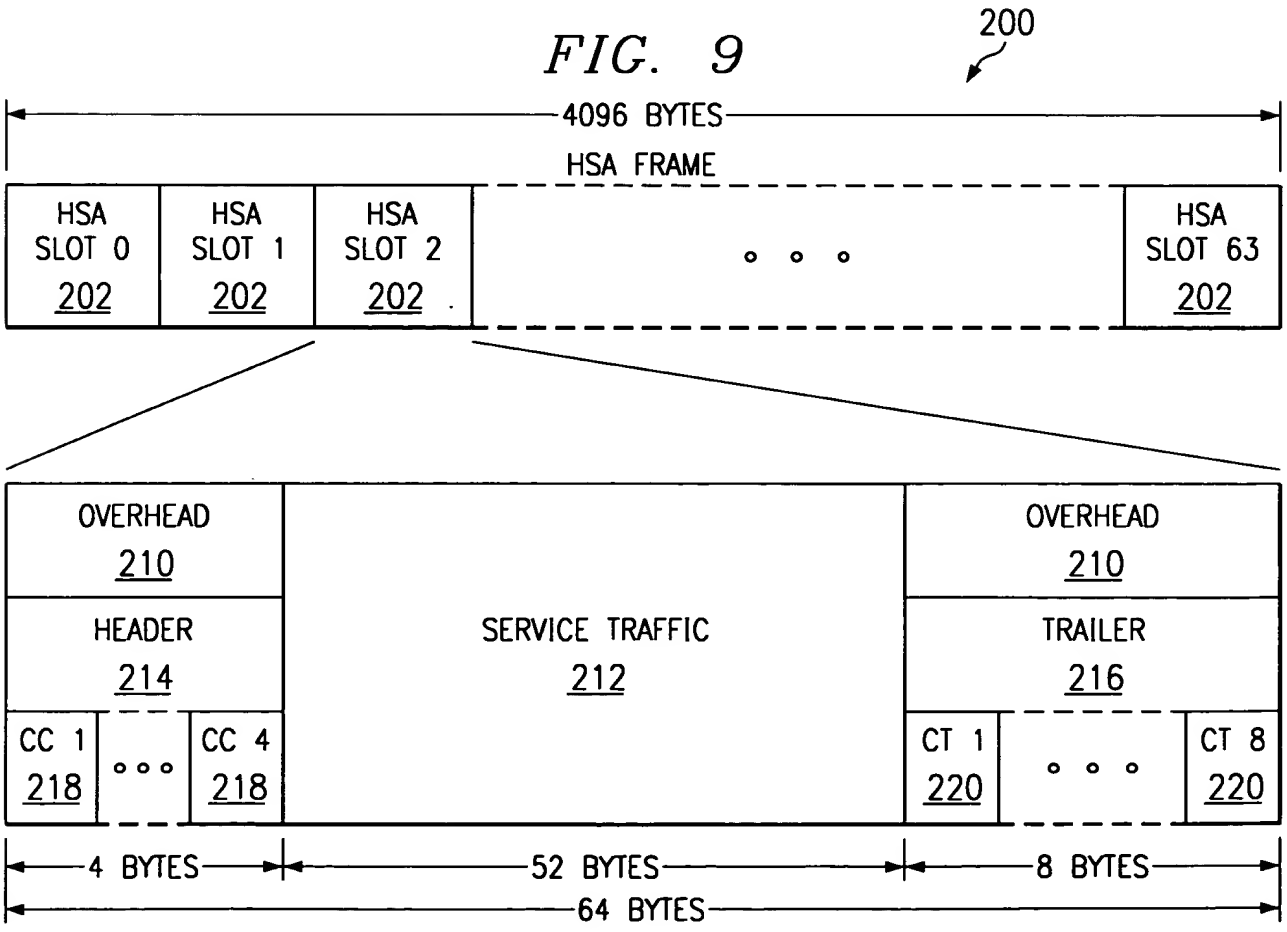

200
4096 BYTES
HSA FRAME
HSA SLOT 0 202
HSA SLOT 1 202
HSA SLOT 2 202
HSA SLOT 63 202
OVERHEAD 210
HEADER 214
CC 1 218
CC 4 218
SERVICE TRAFFIC 212
OVERHEAD 210
TRAILER 216
CT 1 220
CT 8 220
4 BYTES
52 BYTES
8 BYTES
64 BYTES

FIG. 10

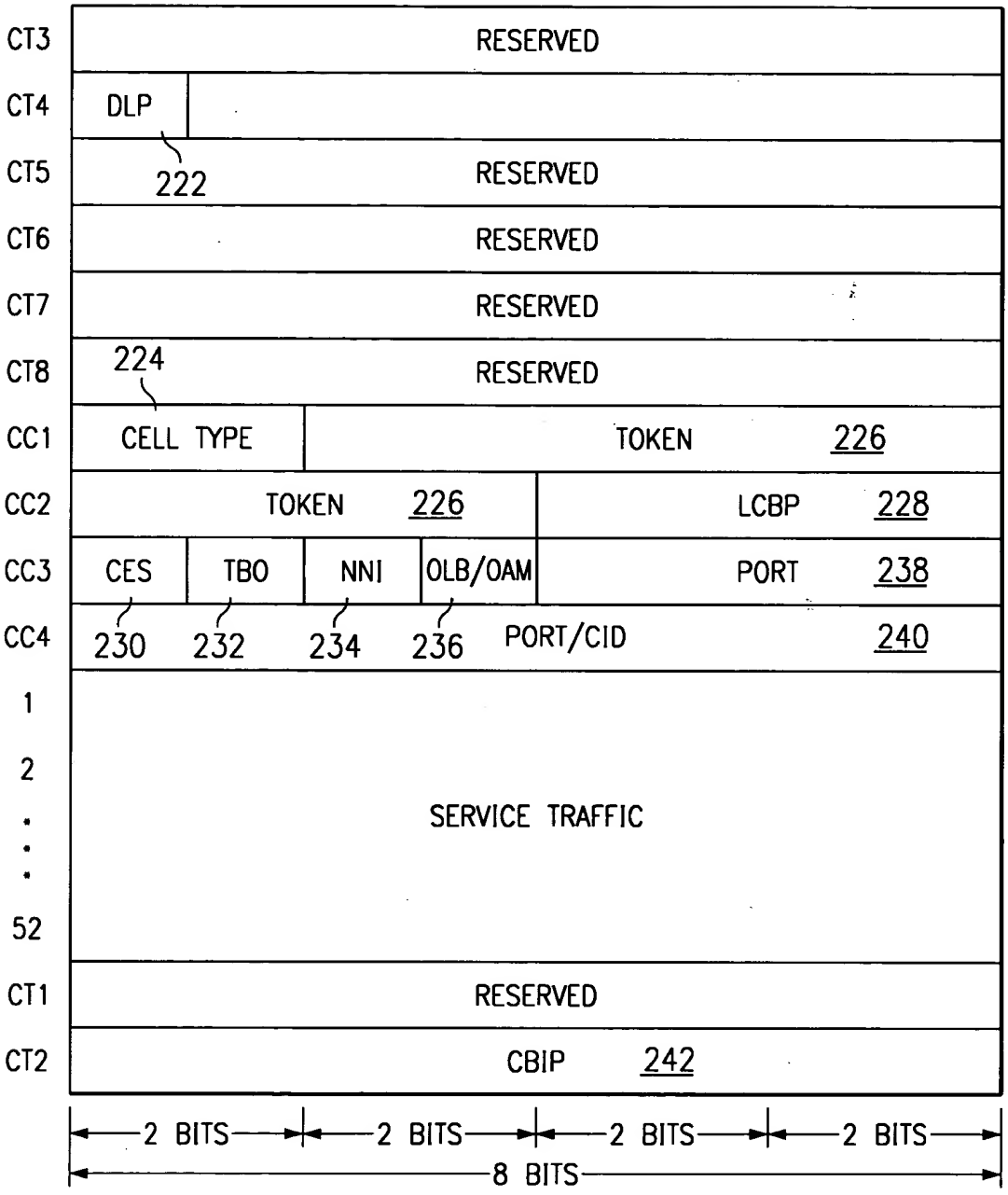

CT3
RESERVED
CT4
DLP
222
CT5
RESERVED
CT6
RESERVED
CT7
RESERVED
CT8
224
RESERVED
CC1
CELL TYPE
TOKEN 226
CC2
TOKEN 226
LCBP 228
CC3
CES
TBO
NNI
OLB/OAM
PORT 238
CC4
230
232
234
236
PORT/CID 240
1
2
52
SERVICE TRAFFIC
CT1
RESERVED
CT2
CBIP 242
2 BITS
2 BITS
2 BITS
2 BITS
8 BITS

FIG. 11

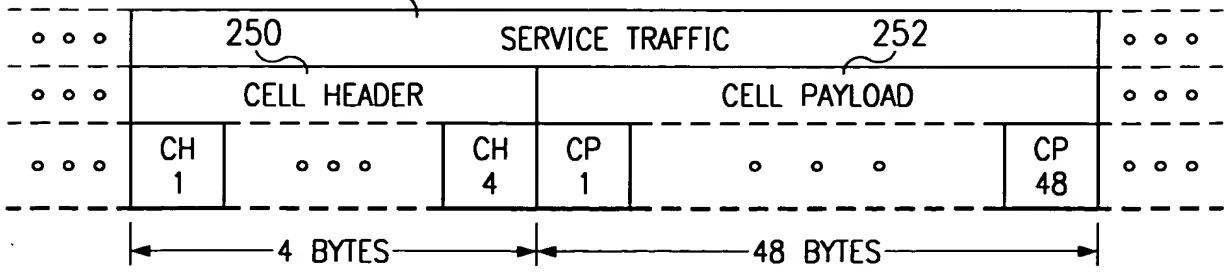

212
250
SERVICE TRAFFIC
252
CELL HEADER
CELL PAYLOAD
CH 1
CH 4
CP 1
CP 48
4 BYTES
48 BYTES

FIG. 12

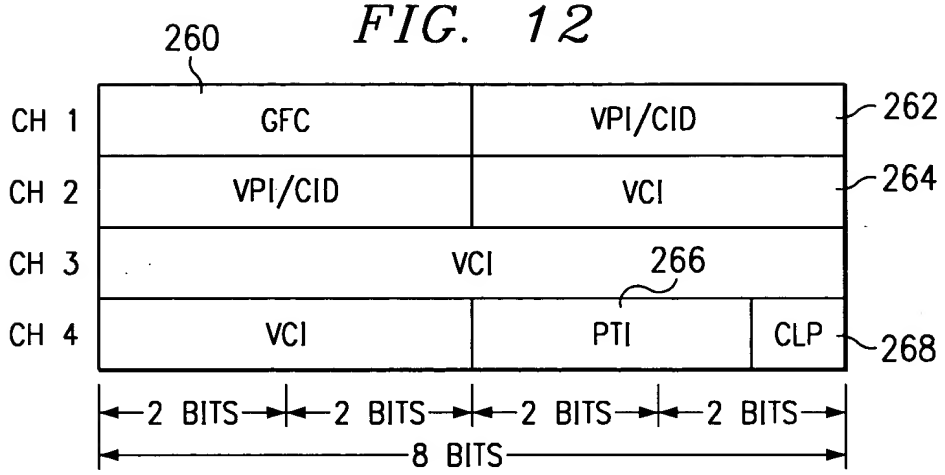

260
CH 1
GFC
VPI/CID
262
CH 2
VPI/CID
VCI
264
CH 3
VCI
266
CH 4
VCI
PTI
CLP
268
2 BITS
2 BITS
2 BITS
2 BITS
8 BITS

FIG. 16

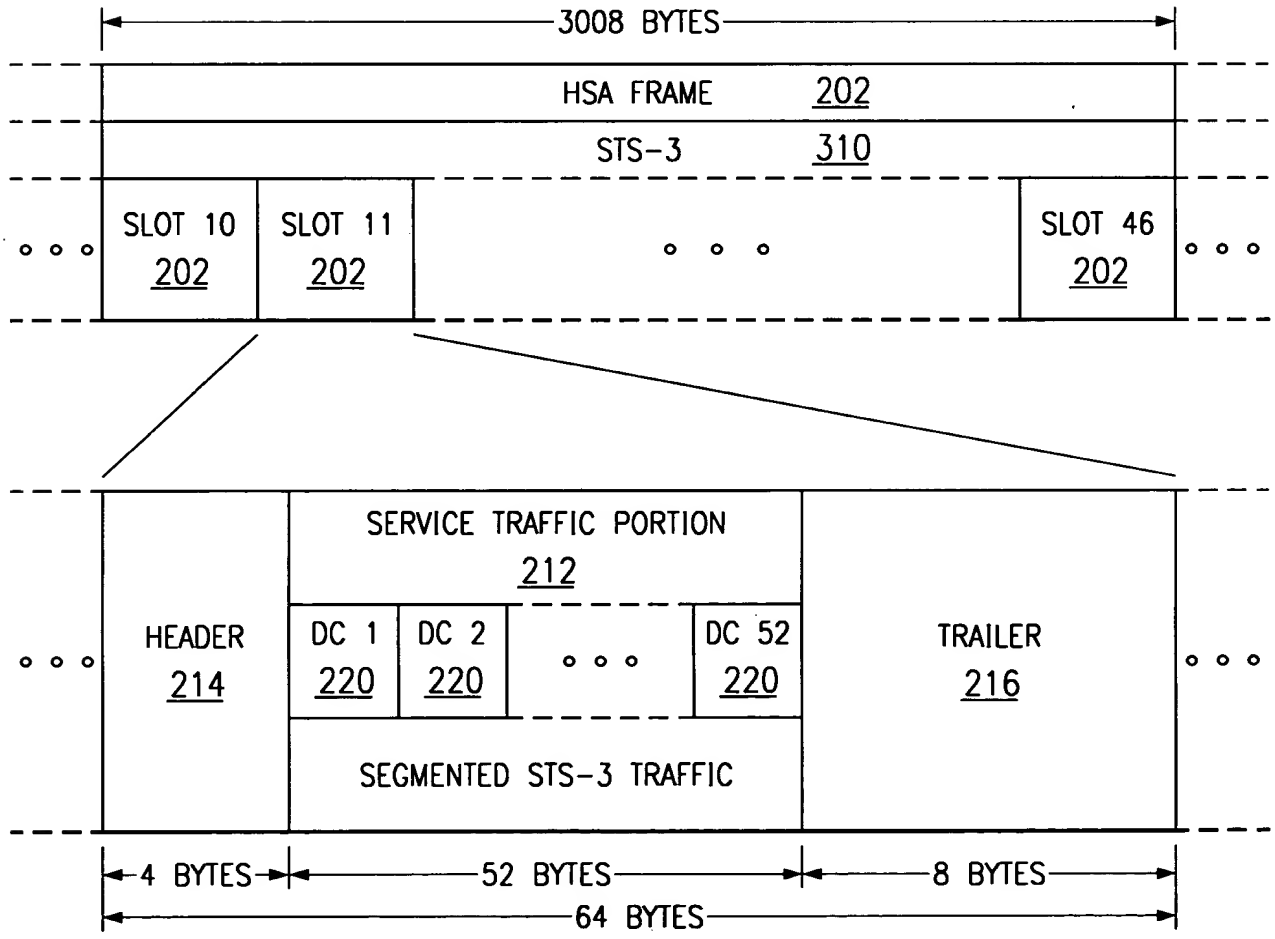

3008 BYTES
HSA FRAME 202
STS-3 310
SLOT 10 202
SLOT 11 202
SLOT 46 202
SERVICE TRAFFIC PORTION 212
HEADER 214
DC 1 220
DC 2 220
DC 52 220
TRAILER 216
SEGMENTED STS-3 TRAFFIC
4 BYTES
52 BYTES
8 BYTES
64 BYTES

FIG. 13

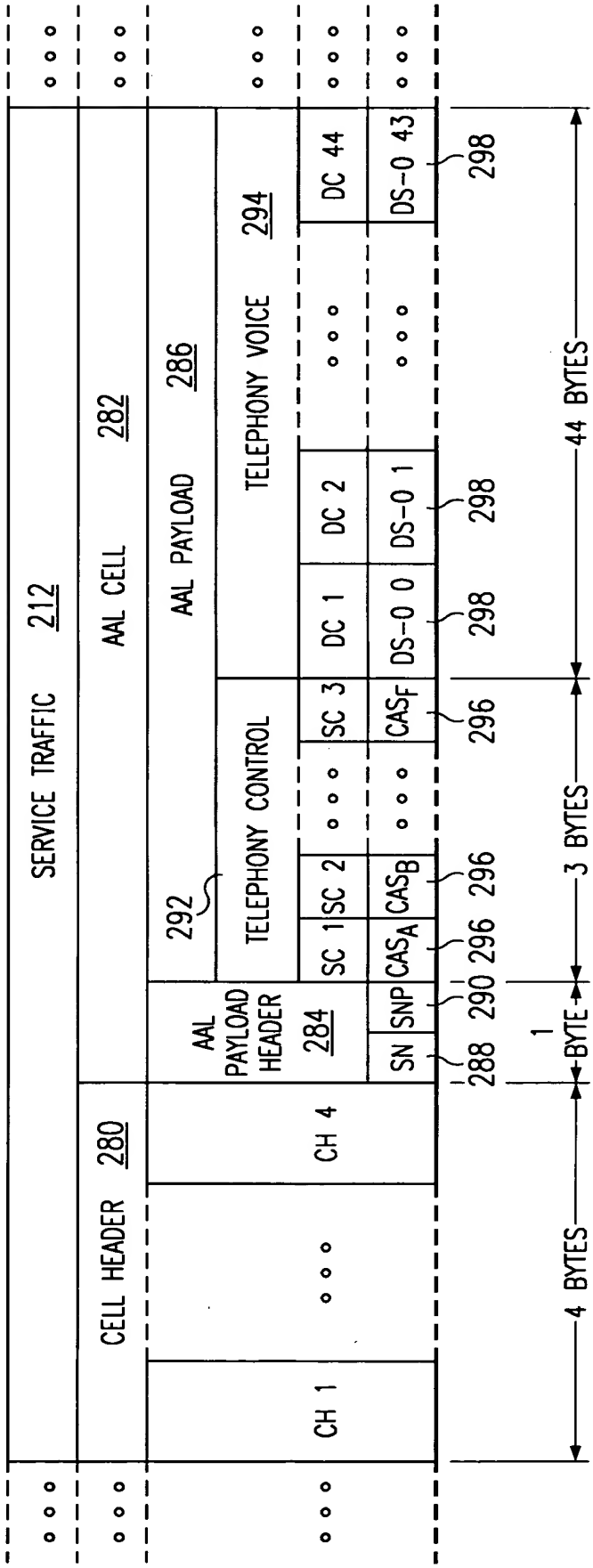

SERVICE TRAFFIC 212
CELL HEADER 280
AAL CELL 282
AAL PAYLOAD 286
AAL PAYLOAD HEADER 284
TELEPHONY CONTROL 292
TELEPHONY VOICE 294
CH 1
CH 4
SN
SNP
SC 1
SC 2
SC 3
DC 1
DC 2
DC 44
DS-0 0
DS-0 1
DS-0 43
CAS_A
CAS_B
CAS_F
288
290
296
298
1 BYTE
3 BYTES
4 BYTES
44 BYTES

FIG. 14

DS0-n VALUE ASSOCIATED WITH CAS_N POSITION TO SN VALUE

SN	CAS_A	CAS_B	CAS_C	CAS_D	CAS_E	CAS_F
0	0	1	2	3	4	5
1	3	4	5	6	7	8
2	6	7	8	9	10	11
3	9	10	11	12	13	14
4	12	13	14	15	16	17
5	15	16	17	18	19	20
6	18	19	20	21	22	23
7	21	22	23	24	25	26
8	24	25	26	27	28	29
9	27	28	29	30	31	32
10	30	31	32	33	34	35
11	33	34	35	36	37	38
12	36	37	38	39	40	41
13	39	40	41	42	43	UNDEF
14	42	43	UNDEF	0	1	2
15	0	1	2	3	4	5

FIG. 15

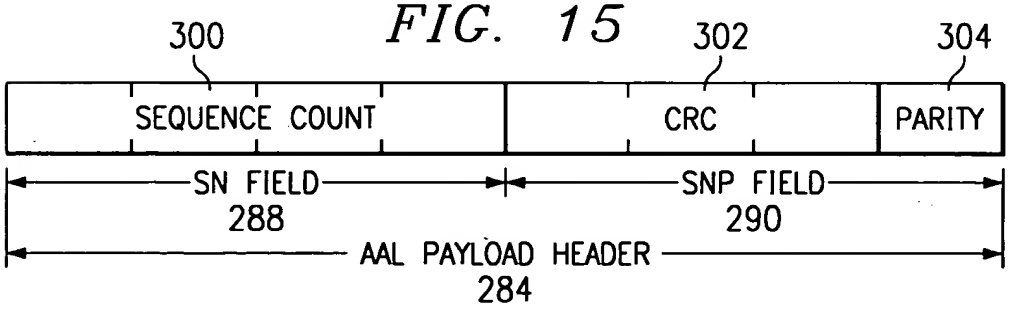


FIG. 17

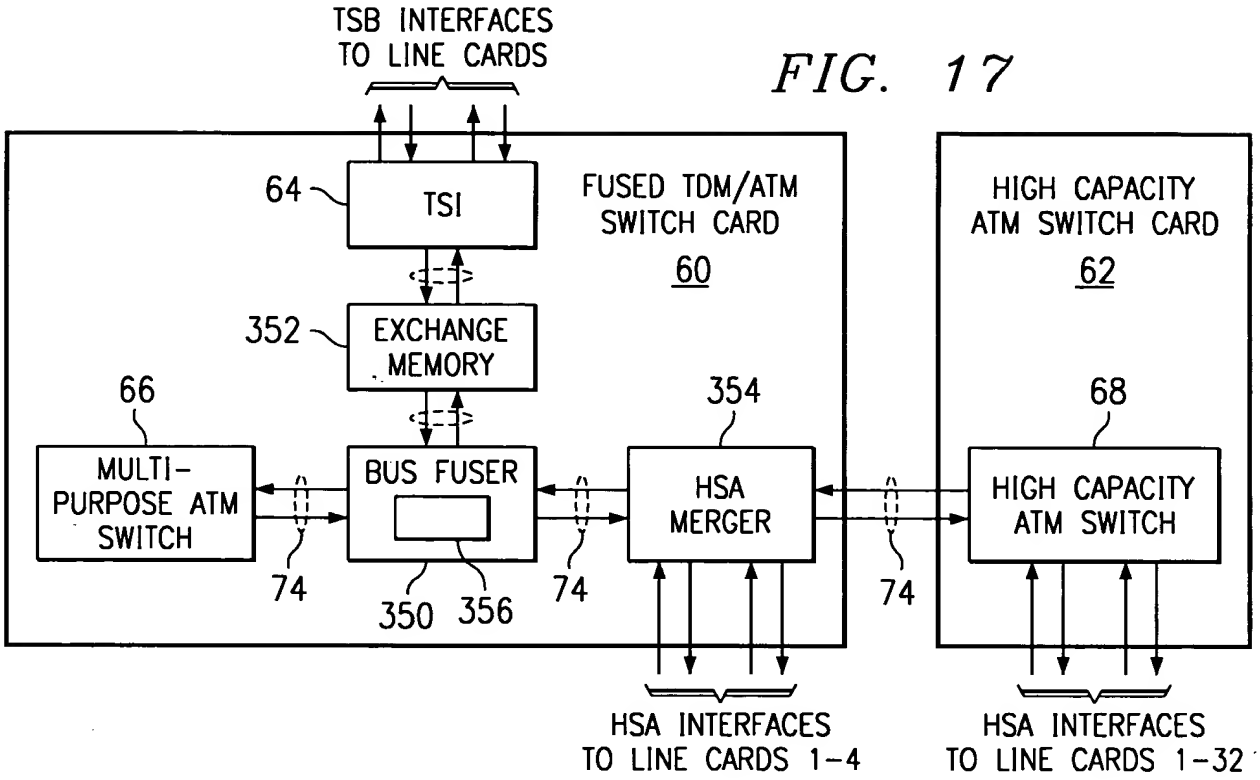
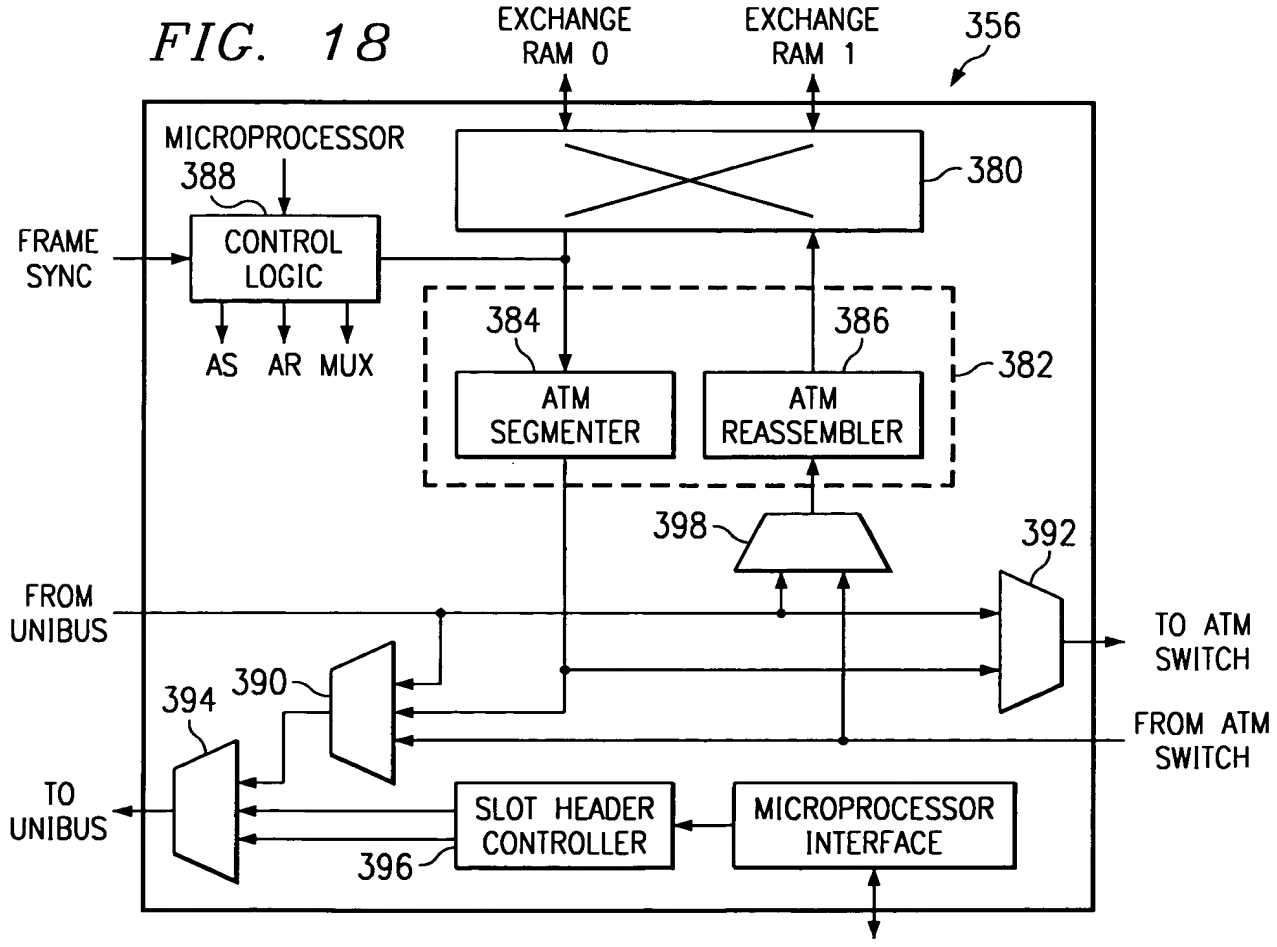

TSB INTERFACES
TO LINE CARDS
64
TSI
FUSED TDM/ATM
SWITCH CARD
60
HIGH CAPACITY
ATM SWITCH CARD
62
352
EXCHANGE
MEMORY
66
354
68
MULTI-
PURPOSE ATM
SWITCH
BUS FUSER
HSA
MERGER
HIGH CAPACITY
ATM SWITCH
74
74
74
350
356
HSA INTERFACES
TO LINE CARDS 1-4
HSA INTERFACES
TO LINE CARDS 1-32

FIG. 18


EXCHANGE
RAM 0
EXCHANGE
RAM 1
356
MICROPROCESSOR
388
380
FRAME
SYNC
CONTROL
LOGIC
AS AR MUX
384
386
382
ATM
SEGMENTER
ATM
REASSEMBLER
398
392
FROM
UNIBUS
TO ATM
SWITCH
394
390
FROM ATM
SWITCH
TO
UNIBUS
SLOT HEADER
CONTROLLER
MICROPROCESSOR
INTERFACE
396

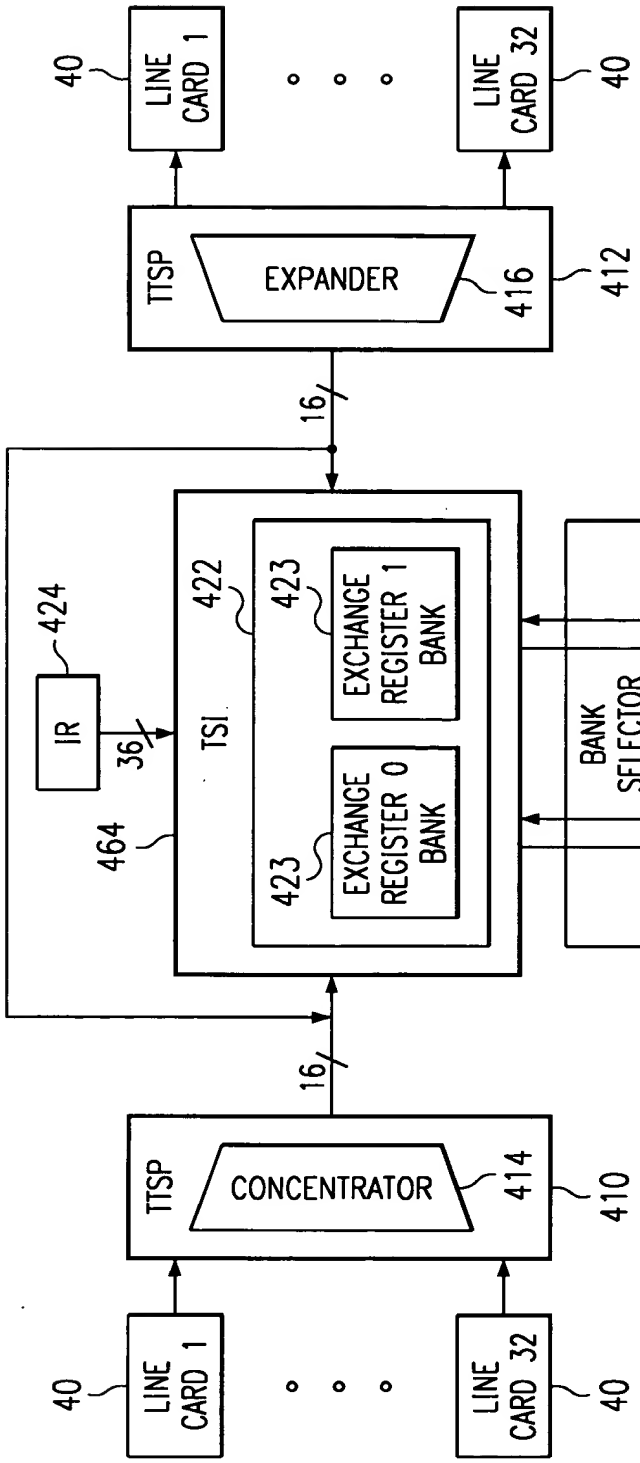

40
LINE CARD 1
LINE CARD 32
40
TTSP
EXPANDER
416
412
16
IR
424
36
464
TSI
422
423
EXCHANGE REGISTER 1 BANK
423
EXCHANGE REGISTER 0 BANK
BANK SELECTOR
EXCHANGE RAM 1
EXCHANGE RAM 0
420
352
16
TTSP
CONCENTRATOR
414
410
40
LINE CARD 1
LINE CARD 32
40

FIG. 19

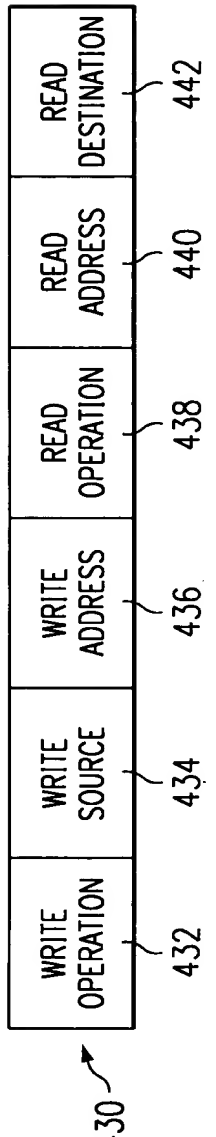

READ DESTINATION
442
READ ADDRESS
440
READ OPERATION
438
WRITE ADDRESS
436
WRITE SOURCE
434
WRITE OPERATION
432
430

FIG. 20

FIG. 21

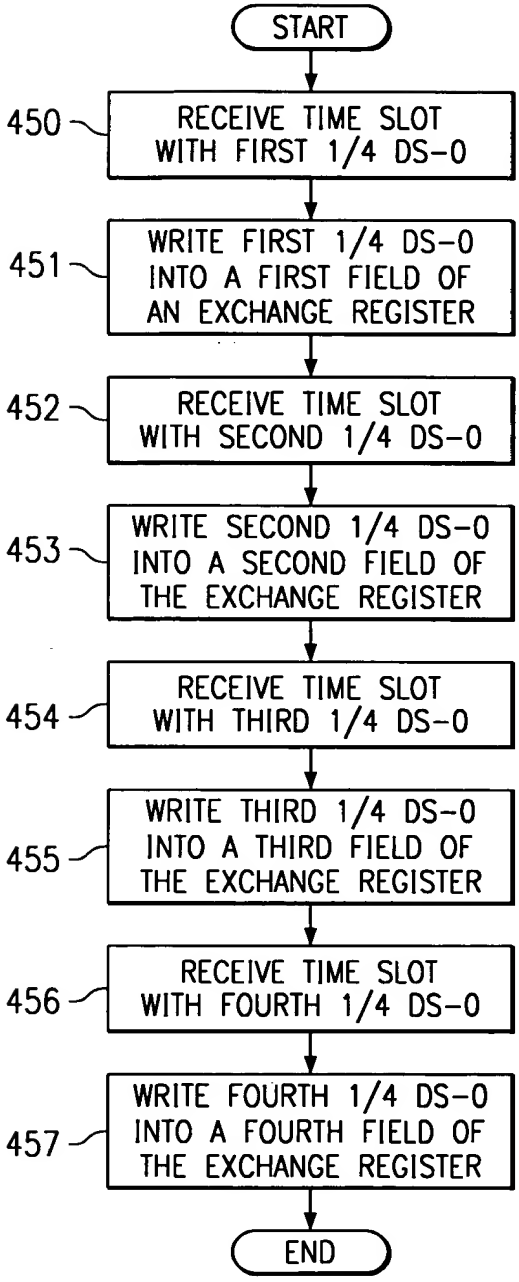

START
450
RECEIVE TIME SLOT WITH FIRST 1/4 DS-0
451
WRITE FIRST 1/4 DS-0 INTO A FIRST FIELD OF AN EXCHANGE REGISTER
452
RECEIVE TIME SLOT WITH SECOND 1/4 DS-0
453
WRITE SECOND 1/4 DS-0 INTO A SECOND FIELD OF THE EXCHANGE REGISTER
454
RECEIVE TIME SLOT WITH THIRD 1/4 DS-0
455
WRITE THIRD 1/4 DS-0 INTO A THIRD FIELD OF THE EXCHANGE REGISTER
456
RECEIVE TIME SLOT WITH FOURTH 1/4 DS-0
457
WRITE FOURTH 1/4 DS-0 INTO A FOURTH FIELD OF THE EXCHANGE REGISTER
END

FIG. 22

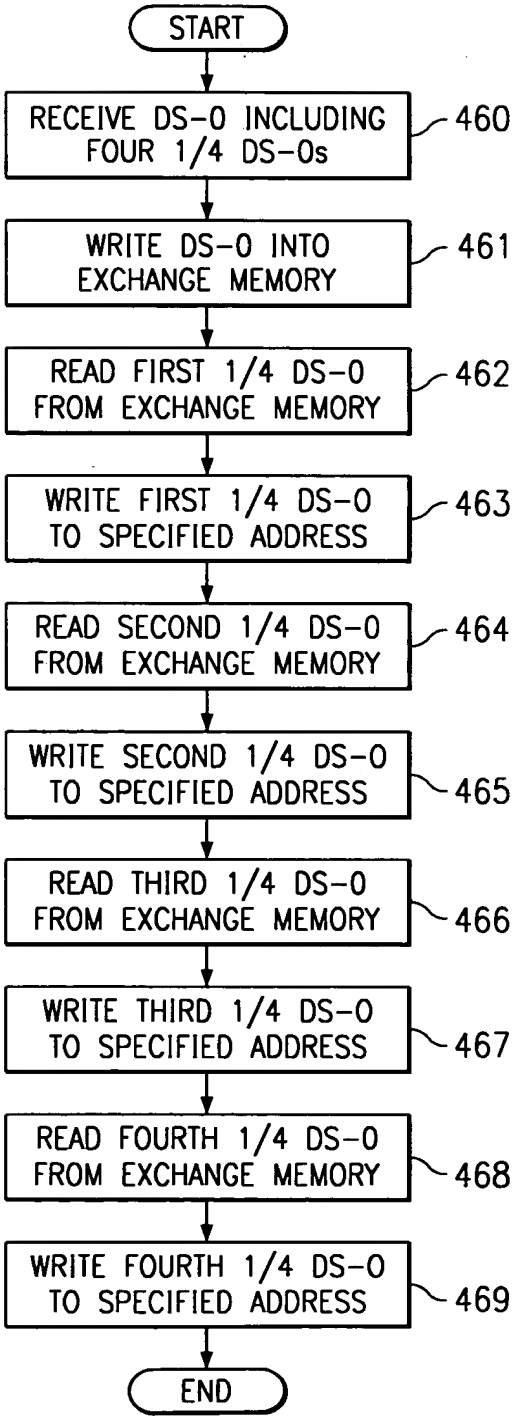

START
RECEIVE DS-0 INCLUDING FOUR 1/4 DS-0s
460
WRITE DS-0 INTO EXCHANGE MEMORY
461
READ FIRST 1/4 DS-0 FROM EXCHANGE MEMORY
462
WRITE FIRST 1/4 DS-0 TO SPECIFIED ADDRESS
463
READ SECOND 1/4 DS-0 FROM EXCHANGE MEMORY
464
WRITE SECOND 1/4 DS-0 TO SPECIFIED ADDRESS
465
READ THIRD 1/4 DS-0 FROM EXCHANGE MEMORY
466
WRITE THIRD 1/4 DS-0 TO SPECIFIED ADDRESS
467
READ FOURTH 1/4 DS-0 FROM EXCHANGE MEMORY
468
WRITE FOURTH 1/4 DS-0 TO SPECIFIED ADDRESS
469
END

FIG. 23

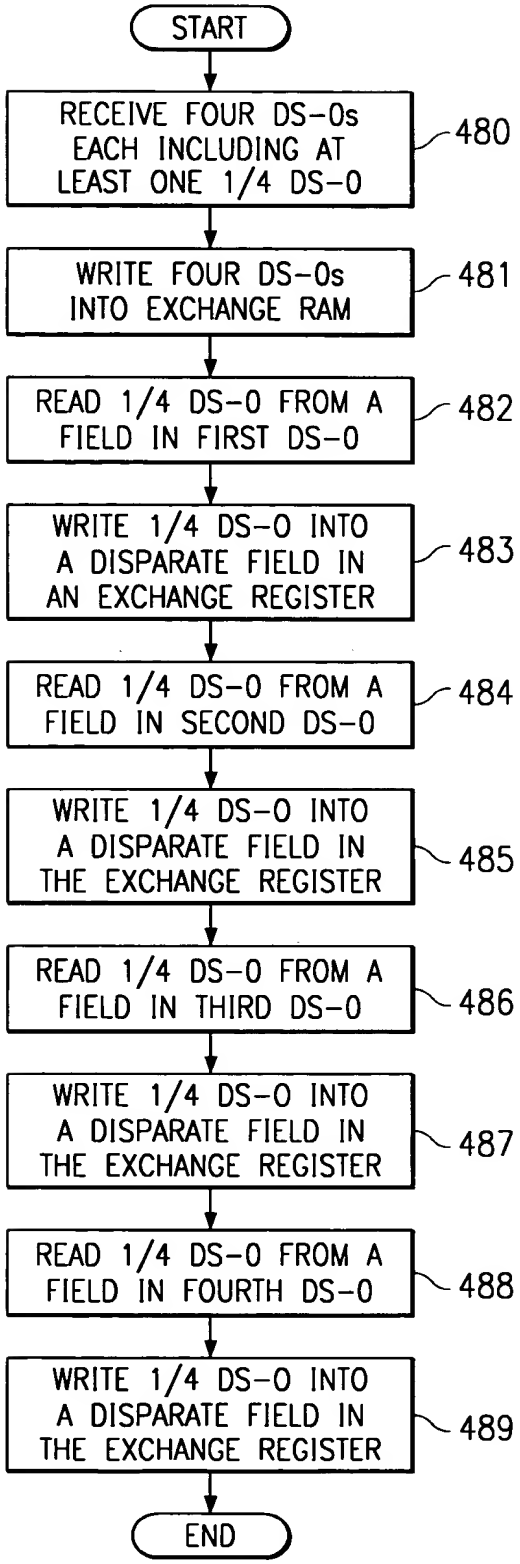

START
RECEIVE FOUR DS-0s EACH INCLUDING AT LEAST ONE 1/4 DS-0
480
WRITE FOUR DS-0s INTO EXCHANGE RAM
481
READ 1/4 DS-0 FROM A FIELD IN FIRST DS-0
482
WRITE 1/4 DS-0 INTO A DISPARATE FIELD IN AN EXCHANGE REGISTER
483
READ 1/4 DS-0 FROM A FIELD IN SECOND DS-0
484
WRITE 1/4 DS-0 INTO A DISPARATE FIELD IN THE EXCHANGE REGISTER
485
READ 1/4 DS-0 FROM A FIELD IN THIRD DS-0
486
WRITE 1/4 DS-0 INTO A DISPARATE FIELD IN THE EXCHANGE REGISTER
487
READ 1/4 DS-0 FROM A FIELD IN FOURTH DS-0
488
WRITE 1/4 DS-0 INTO A DISPARATE FIELD IN THE EXCHANGE REGISTER
489
END

FIG. 24

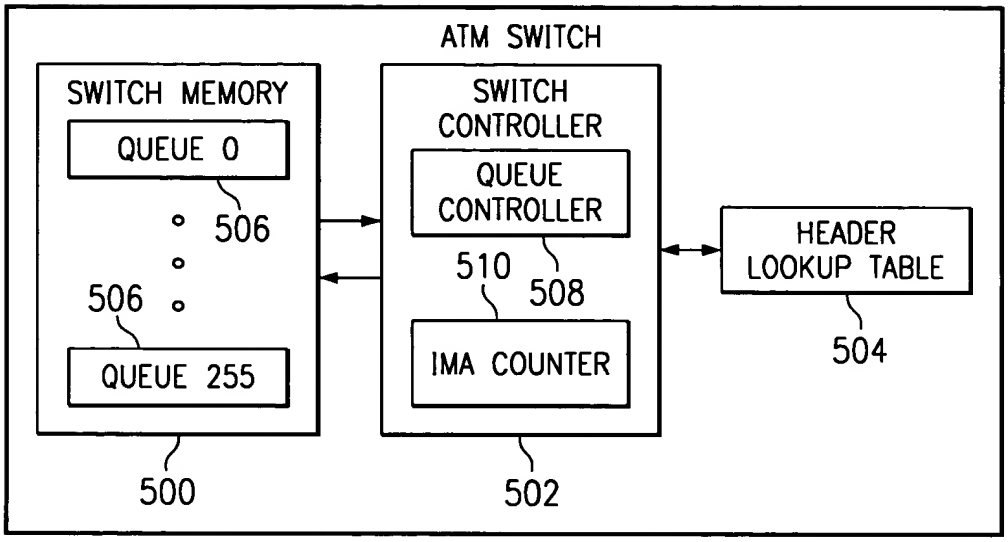


FIG. 25

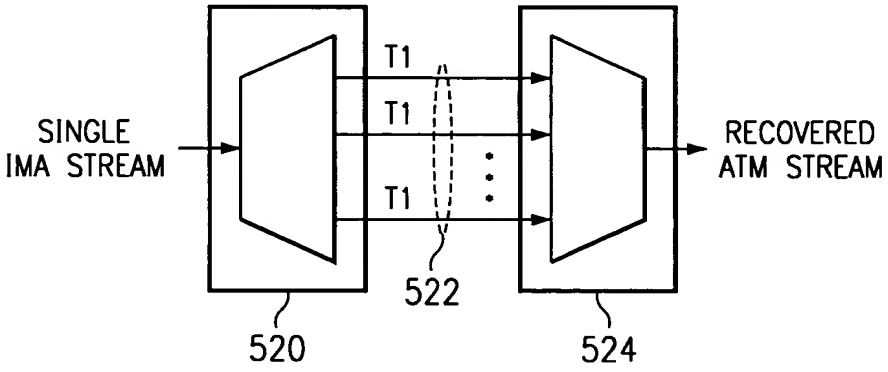


FIG. 28

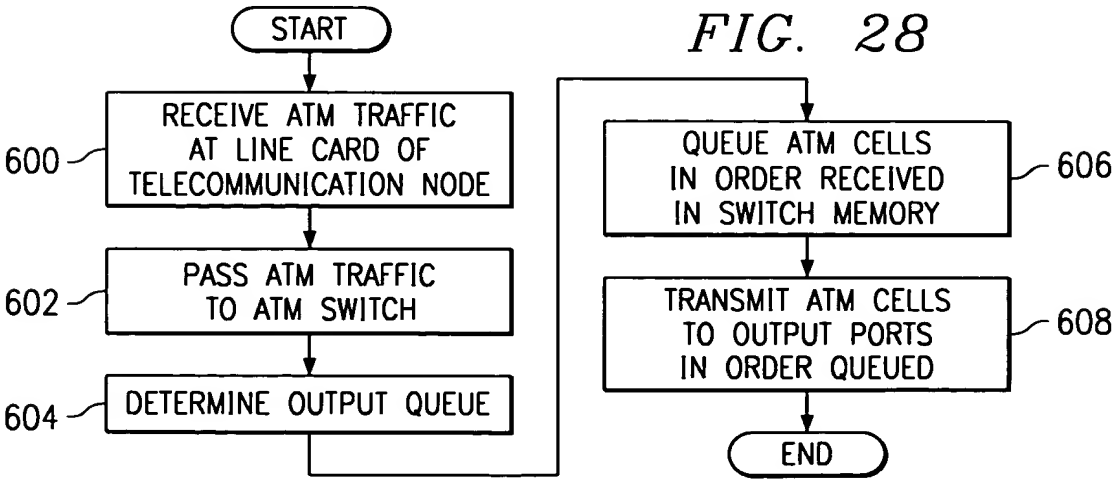


FIG. 26

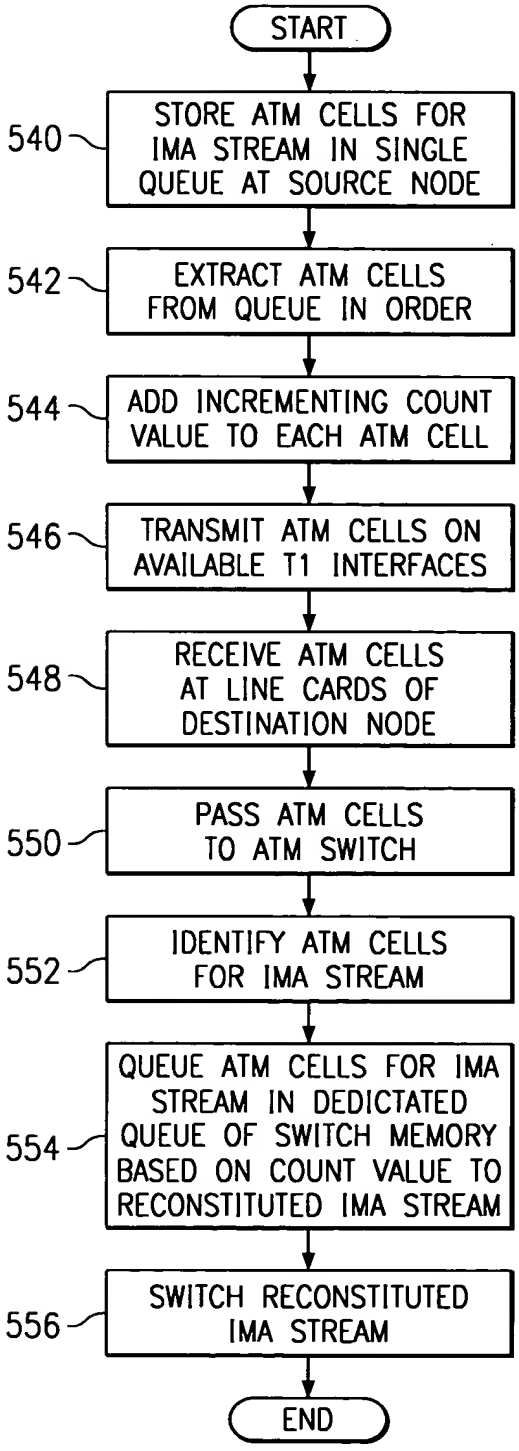
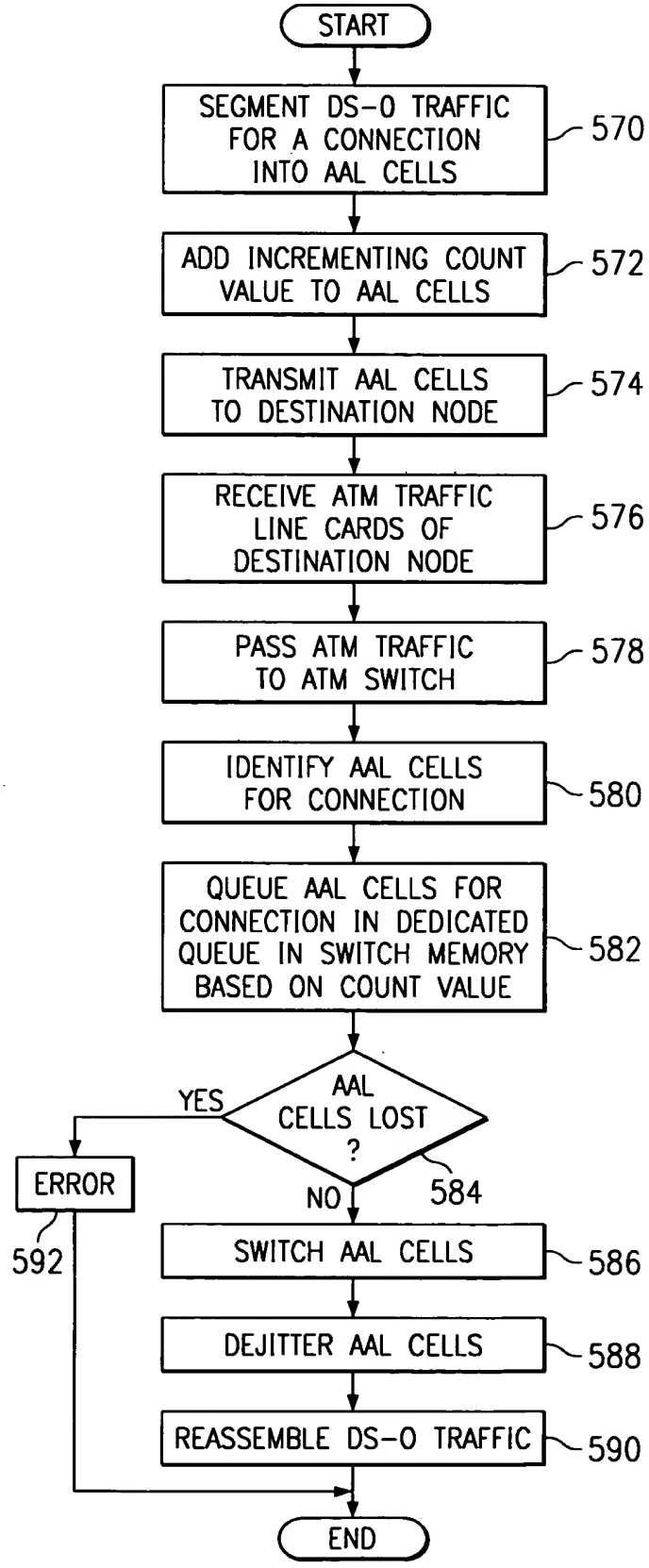

START
STORE ATM CELLS FOR IMA STREAM IN SINGLE QUEUE AT SOURCE NODE
540
EXTRACT ATM CELLS FROM QUEUE IN ORDER
542
ADD INCREMENTING COUNT VALUE TO EACH ATM CELL
544
TRANSMIT ATM CELLS ON AVAILABLE T1 INTERFACES
546
RECEIVE ATM CELLS AT LINE CARDS OF DESTINATION NODE
548
PASS ATM CELLS TO ATM SWITCH
550
IDENTIFY ATM CELLS FOR IMA STREAM
552
QUEUE ATM CELLS FOR IMA STREAM IN DEDICTATED QUEUE OF SWITCH MEMORY BASED ON COUNT VALUE TO RECONSTITUTED IMA STREAM
554
SWITCH RECONSTITUTED IMA STREAM
556
END

FIG. 27


START
SEGMENT DS-0 TRAFFIC FOR A CONNECTION INTO AAL CELLS
570
ADD INCREMENTING COUNT VALUE TO AAL CELLS
572
TRANSMIT AAL CELLS TO DESTINATION NODE
574
RECEIVE ATM TRAFFIC LINE CARDS OF DESTINATION NODE
576
PASS ATM TRAFFIC TO ATM SWITCH
578
IDENTIFY AAL CELLS FOR CONNECTION
580
QUEUE AAL CELLS FOR CONNECTION IN DEDICATED QUEUE IN SWITCH MEMORY BASED ON COUNT VALUE
582
AAL CELLS LOST ?
584
YES
NO
ERROR
592
SWITCH AAL CELLS
586
DEJITTER AAL CELLS
588
REASSEMBLE DS-0 TRAFFIC
590
END

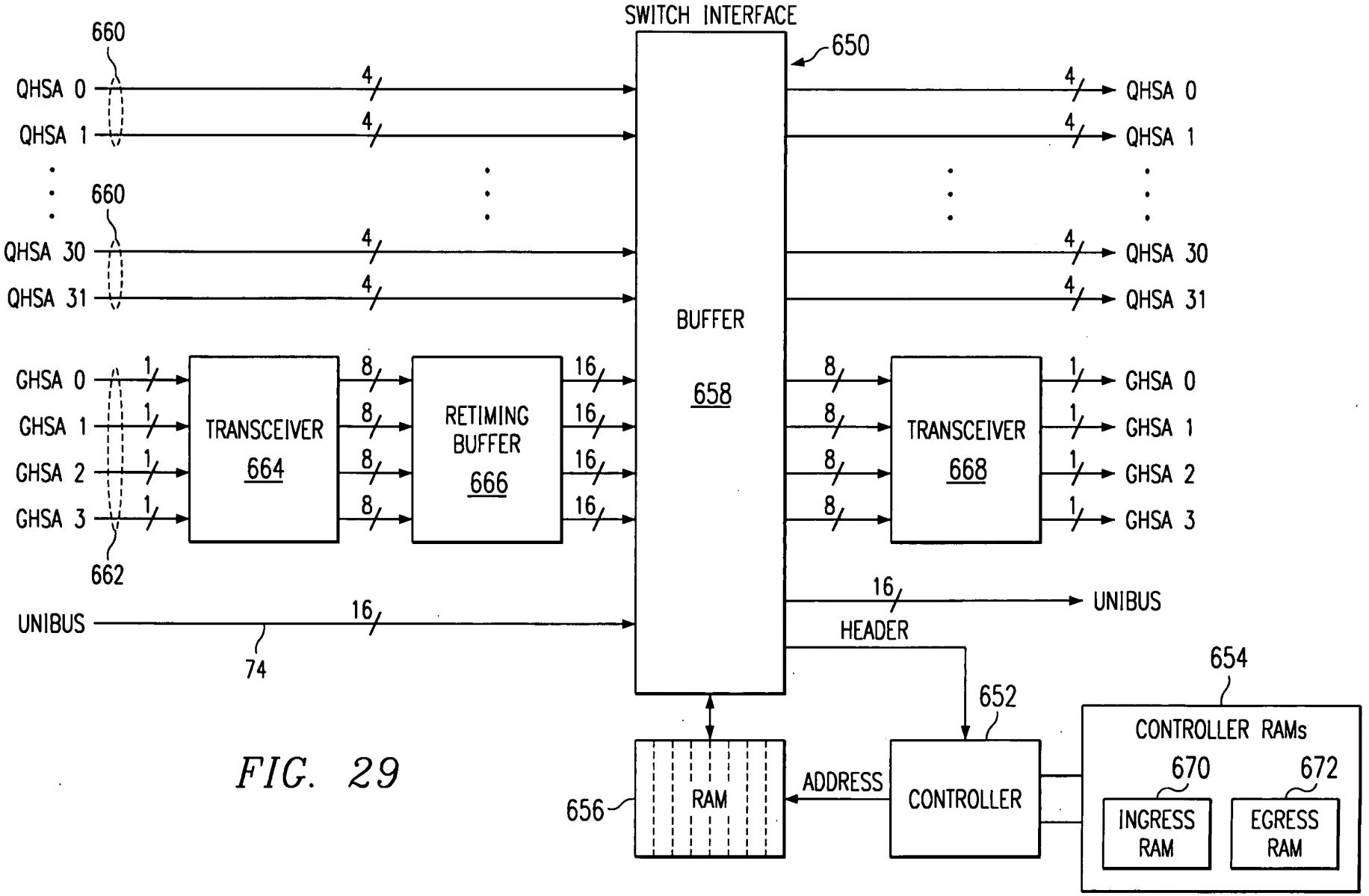

SWITCH INTERFACE
650
660
QHSA 0
QHSA 1
660
QHSA 30
QHSA 31
4
BUFFER
658
GHSA 0
GHSA 1
GHSA 2
GHSA 3
1
TRANSCEIVER
664
8
RETIMING
BUFFER
666
16
662
UNIBUS
16
74
TRANSCEIVER
668
16
UNIBUS
HEADER
652
654
CONTROLLER RAMs
670
672
INGRESS
RAM
EGRESS
RAM
CONTROLLER
ADDRESS
RAM
656

FIG. 29

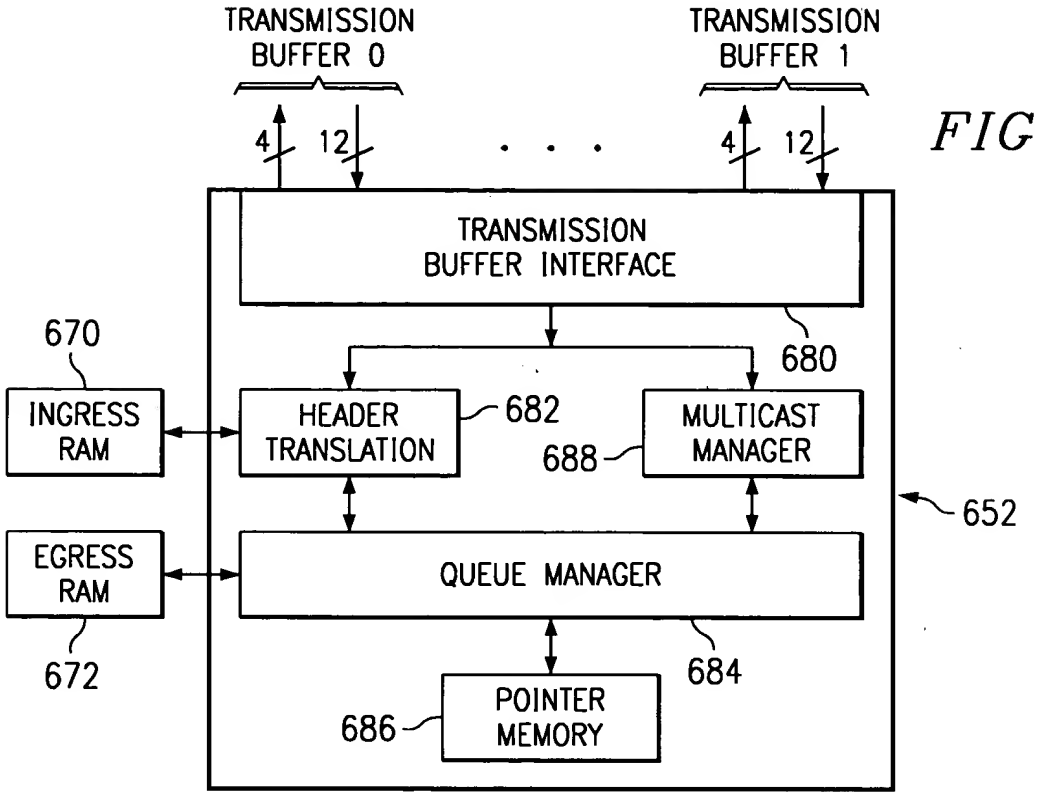


FIG. 30

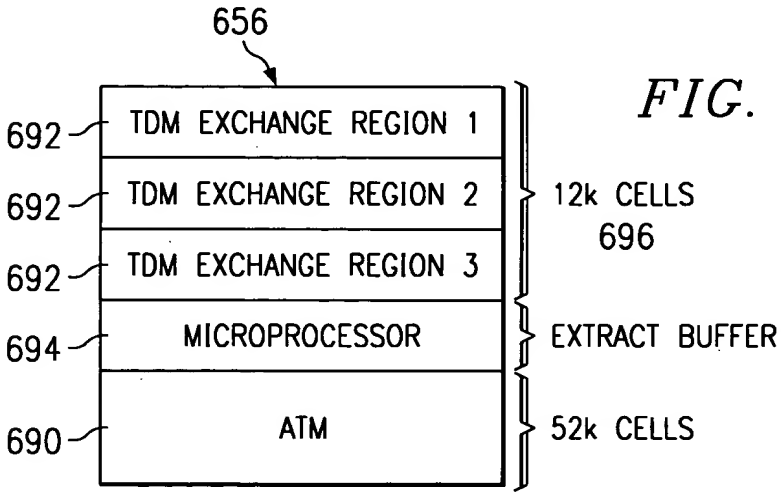


FIG. 31

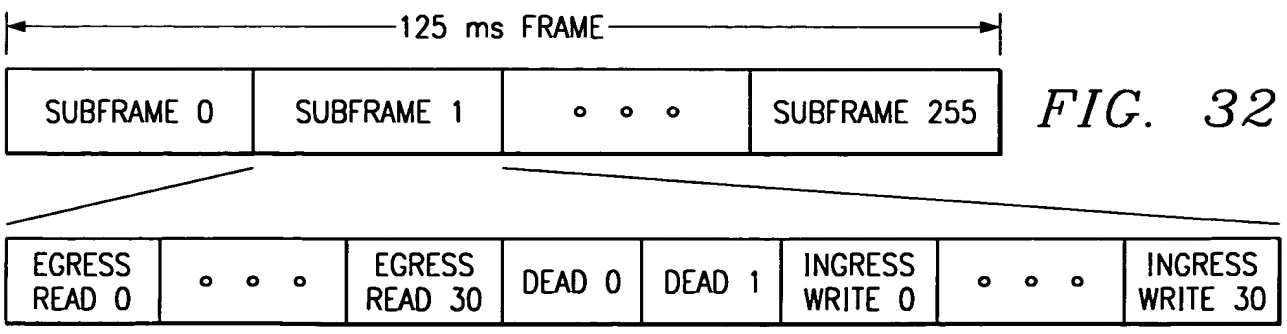


FIG. 32

FIG. 33

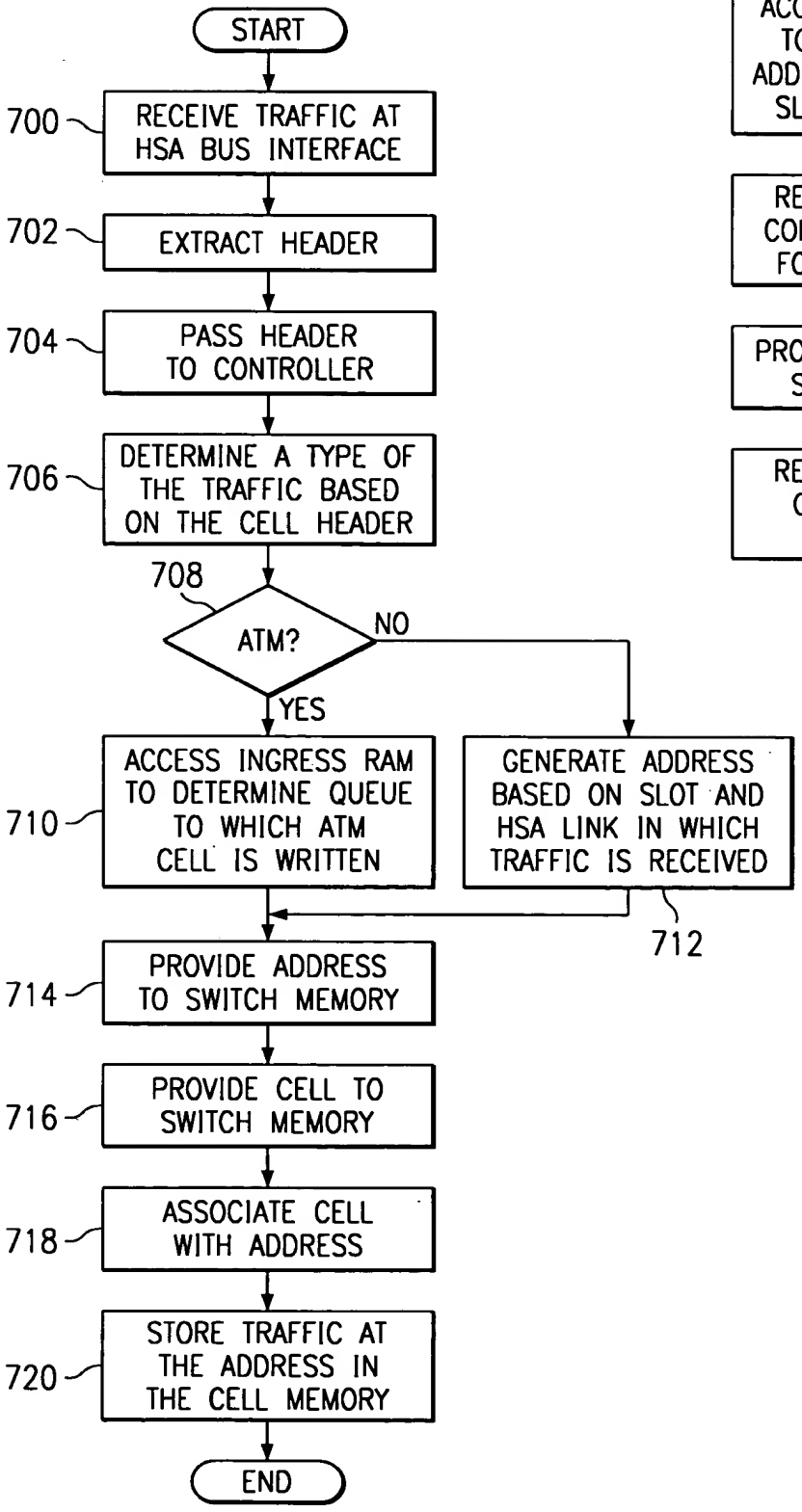
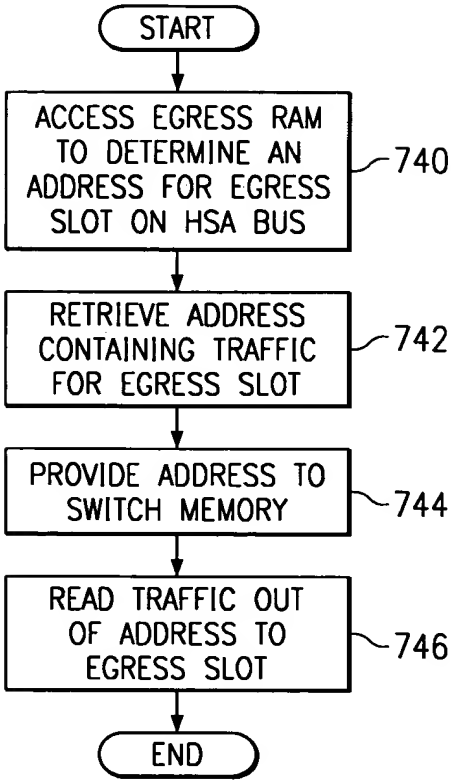

START
700
RECEIVE TRAFFIC AT HSA BUS INTERFACE
702
EXTRACT HEADER
704
PASS HEADER TO CONTROLLER
706
DETERMINE A TYPE OF THE TRAFFIC BASED ON THE CELL HEADER
708
ATM?
NO
YES
710
ACCESS INGRESS RAM TO DETERMINE QUEUE TO WHICH ATM CELL IS WRITTEN
GENERATE ADDRESS BASED ON SLOT AND HSA LINK IN WHICH TRAFFIC IS RECEIVED
712
714
PROVIDE ADDRESS TO SWITCH MEMORY
716
PROVIDE CELL TO SWITCH MEMORY
718
ASSOCIATE CELL WITH ADDRESS
720
STORE TRAFFIC AT THE ADDRESS IN THE CELL MEMORY
END

FIG. 34


START
ACCESS EGRESS RAM TO DETERMINE AN ADDRESS FOR EGRESS SLOT ON HSA BUS
740
RETRIEVE ADDRESS CONTAINING TRAFFIC FOR EGRESS SLOT
742
PROVIDE ADDRESS TO SWITCH MEMORY
744
READ TRAFFIC OUT OF ADDRESS TO EGRESS SLOT
746
END